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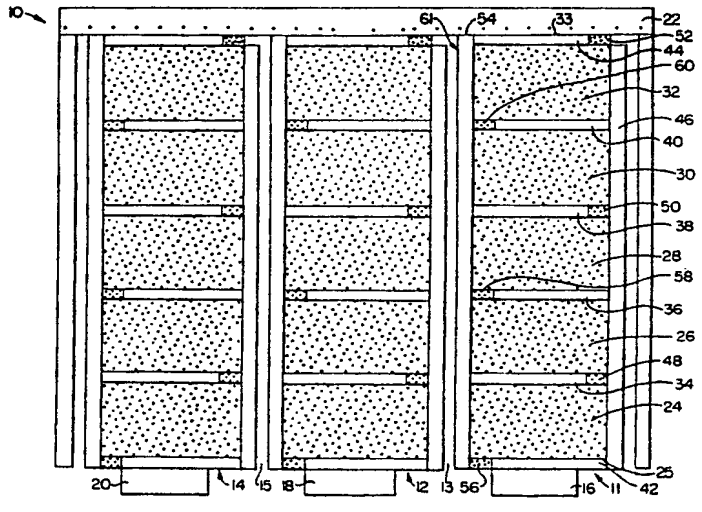
(54) Title: TWO-DIMENSIONAL ARRAY ULTRASONIC TRANSDUCERS

(57) Abstract

A piezoelectric transducer chip (10) comprising a plurality of transducer elements (11, 12, 14) arranged in a two-dimensional array is disclosed. At leat one of the transducer elements is a multi-layer element which comprises a plurality of piezoelectric layers (24, 26, 28, 30, 32), each of which is separated from the adjacent piezoelectric layers by an electrode layer (34, 36, 38, 40) so that a plurality of capacitive elements is electrically connected in parallel. A first via (46) connects a first set of alternating electrode layers, and a second via (54) connects a second set of alternating electrode layers. The first via is insulated from the second set of alternating electrode layers, and the second via is insulated from the first set of alternating electrode layers. At least one of the plurality of multi-layer elements has an internal edge. At least one of the vias of a multi-layer element is an internal via. Also disclosed are an ultrasonic transducer (11) which includes such a piezoelectric chip, and an ultrasonic scanner (140) which includes such a transducer.



INTERNATIONAL SEARCH REPORT

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,773,140 (McAusland) 27 November 1988, See entire document.	1-20
A	US, A, 4,755,708 (Granz et al) 05 July 1988, See entire document.	1-20
A	US,A, 4,747,192 (Rokurota) 31 May 1988, See entire document	1-20
A	US,A, 4,890,268 (Smith et al) 26 December 1989, See entire document.	1-20
A	US, A, 4,945,915 (Nagasaki et al) 07 August 1990, See entire document	1-20
A	US,A, 4,958,227 (Saitoh et al) 18 September 1990, See entire document.	1-20
A	US,A, 5,014,711 (Nagasaki et al) 14 May 1991, See entire document.	1-20
A	US,A, 5,045,746 (Wersing et al) 03 September 1991, See entire document.	1-20
A	US,A, 5,091,893 (Smith et al) 25 February 1991, See entire document.	1-20
A	US,A, 4,865,042 (Umemura et al) 12 September 1989, See enitre document	1-20

TWO-DIMENSIONAL ARRAY ULTRASONIC TRANSDUCERS

Field of the Invention

This application relates generally to the fields of medical diagnostic ultrasound, underwater acoustic imaging, and the associated piezoelectric transducers, and more specifically relates to two-dimensional arrays with multi-layer transducer elements.

Background of the Invention

Diagnostic ultrasound is an essential modality in virtually every medical specialty and particularly in obstetrics, cardiology and radiology. The ultrasound transducer is the critical component and the limiting factor affecting the quality of diagnostic ultrasound imaging and Doppler measurements. In a conventional circular piston piezoelectric transducer used in mechanical scanning for medical applications (e.g., 19mm diameter, 3.5MHz resonant frequency) the electrical impedance of the transducer is approximately 50Ω. Such a transducer is well matched to the conventional electrical transmit circuit for delivering large amounts of acoustic power to the tissue load during the transmit mode. In a like manner, in receive mode, such a transducer is well suited for driving the typical 50Ω or

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vibrations from the desired transducer pass band. Adherence to these performance characteristics have produced linear arrays having long narrow elements which are sized to be less than one wavelength wide for the ultrasonic frequencies used in tissue imaging, (e.g., <0.3mm wide x 10mm long at 3.5 MHz).

Two dimensional (NxM) transducer arrays are believed to hold promise in improving clinical image quality in future diagnostic ultrasound equipment. An immediate clinical application of 2-D phased arrays is the reduction of image slice thickness by focusing in the elevation plane perpendicular to the scanning dimension. An additional application of 2-D transducer arrays is the correction of phase aberrations introduced across the transducer aperture by tissue inhomogeneities. These aberrations occur in two dimensions, so 2-D arrays combined with the proper phase correction signal processing can restore diagnostic image quality. In addition to improving conventional ultrasound B-scan image quality, two-dimensional transducer arrays should assist in the development of new modes of ultrasound imaging. Projected new techniques include: (1) presentation of simultaneous orthogonal B-mode scans; (2) acquisition of several B-scans electronically steered in the elevation direction; (3) development of high-speed C-scans; and (4) high-speed volumetric ultrasound scanning to enable real time three-dimensional imaging and volumetric, angle-independent flow imaging. With known technology, these techniques can only be implemented with 2-D array transducers.

Unfortunately, the design and fabrication problems of one-dimensional transducer arrays become almost overwhelming when extended to a two dimensional array, in which case the element size may be less than 0.2mm x 0.2mm for more than 1000 elements in the array. There are two significant obstacles which limit the use of 2-D transducer arrays. First, a simple fabrication

method for the electrical connections to such array elements, which can be less than one ultrasound wavelength on a side, is not known. Second, it is very difficult to achieve adequate sensitivity and bandwidth from such small elements.

In the last 15 years there have been several descriptions of prototype 2-D array transducers for medical ultrasonic imaging, but the resulting products were acoustically unsuitable for modern medical ultrasound imaging procedures.

Two dimensional arrays also have been confronted with the problem of high electrical impedance in transducer elements. Two-dimensional arrays have been developed in two geometries. A typical geometry for a 4 x 32 array transducer ia designed for focusing (but not steering) in the elevation direction and for correction of phase aberrations in two dimensions. Such transducers have been called 1.5-D arrays. For a transducer array of this design, each element typically exhibits complex impedance, the magnitude of which is approximately 1000Ω at a resonance of 3.5MHz; this complex impedance causes an electrical impedance mismatch and the accompanying sensitivity decrease which are more severe than seen in linear arrays. Elements in full 2-D arrays which can steer the ultrasound beam in azimuth as well as elevation may be smaller than 0.2mm x 0.2mm; these elements exhibit a complex electrical impedance having a magnitude of approximately 5000Ω or greater, so sensitivity is further reduced. Thus, for 1.5-D and 2-D arrays, the development of suitable piezoelectric materials are critical to improved sensitivity.

Unfortunately, the piezoelectric ceramics as described in the prior art are ill suited for such transducers. 1.5-D and 2-D arrays are commonly fabricated by dicing a single piezoelectric chip in two directions with a kerf width as small as .01mm. In the prior art, termination electrodes for parallel electrical

connection of the alternate layers can only be placed on the external edges of the piezoelectric chip as described by Saitoh et al. Thus, after dicing, elements in the inner rows and columns of 1.5-D and 2-D arrays have no side electrodes.

In an attempt to address the problem of high electrical impedance in linear arrays, U.S. Patent No. 4,958,327 to Saitoh et al., teaches the concept of a multi-layer ceramic piezoelectric material consisting of K layers laminated in parallel electrically but in series acoustically. For K layers of uniform thickness, the capacitance of each element is increased by K^2; this capacitive increase reduces the electrical impedance of the element by K^2 and significantly improving transmit efficiency and receive mode sensitivity. However, the teaching of Saitoh is inapplicable to two dimensional arrays; as the electrode layers are short circuited on a side surface of element, the concept is limited to elements with electrode layers having a surface on the periphery of the transducer, and cannot be used for the elements of the inner rows of two dimensional arrays.

In view of the foregoing, it is an object of the present invention to provide a two-dimensional ultrasound transducer chip which includes multilayer elements in the inner rows of the arrays.

It is a further object of the invention to provide an ultrasound transducer array which contains such a transducer chip.

It is an additional object of the invention to provide ultrasound diagnostic devices which utilize a two-dimensional transducer array as described.

Summary of the Invention

These and other objects are satisfied by the present invention, which includes as a first aspect a piezoelectric transducer chip comprising a plurality of transducer elements arranged in a two-dimensional array. At least one of the transducer elements is a multi-layer

element which comprises a plurality of piezoelectric layers, each of which is separated from the adjacent piezoelectric layers by an electrode layer so that a plurality of capacitive elements electrically connected in parallel. A first via connects a first set of alternating electrode layers, and a second via connects a second set of alternating electrode layers. The first via is insulated from the second set of alternating electrode layers, and the second via is insulated from the first set of alternating electrode layers. At least one of the plurality of multi-layer elements has an internal edge. At least one of the vias of a multi-layer element is an internal via.

A second aspect of the present invention is an ultrasonic transducer array utilizing a two-dimensional piezoelectric chip as described above. The transducer array comprises the 2-D chip, a connector having an array of connector pads for electrically connecting the connector to the chip, means for electrically connecting a first set of alternating electrode layers of the chip to ground, and means for electrically connecting a second set of alternating electrode layers of the chip to a corresponding one of the connector pads.

A third aspect of the invention is an ultrasonic scanner utilizing the 2-D chip. The scanner comprises means for producing an ultrasonic signal, an ultrasonic transducer array of which includes the 2-D chip, means for amplifying a received ultrasonic signal, and means for processing and displaying the ultrasonic signal. In a preferred embodiment, the scanner is a medical diagnostic tool for ultrasonic scanning of tissue.

Brief Description of the Drawings

Figure 1 is a side cross-sectional view of a 3x3 two dimensional transducer array with five piezoelectric layers.

Figure 2 is a top view of a 3x3 two dimensional transducer array.

Figure 3A is a top section view of a two dimensional array having split vias taken through an electrode layer of a first set of alternating electrode layers.

Figure 3B is a top section view of a two dimensional array having split vias taken through an electrode layer of a second set of alternating electrode layers interposed between the first set of electrode layers of **Figure 3A**.

Figure 4 is a side cross-sectional view of a 3x3 two dimensional transducer array with two elements having five piezoelectric layers and one single layer element.

Figure 5 is a cross-sectional view of a two-dimensional array including an upper stand-off for improved image quality obtained by direct contact of the transducer on a subject's skin.

Figure 6 is a top view of the footprint of a transducer to be incorporated into a handle for easier use.

Figure 7 is a bottom view of the transducer of **Figure 6** showing wider interelement spacing.

Figure 8 is a block diagram showing the electrical connections of an ultrasonic scanner for medical diagnostic use.

Detailed Description of the Invention

The present invention provides a two-dimensional ultrasound transducer array having improved sensitivity with small transducer elements. It does so by providing a transducer chip with multiple piezoelectric layers which can be fabricated using multi-layer ceramic (MLC) technology. Alternate piezoelectric layers are electrically connected through the use of "vias."

An exemplary embodiment of a transducer chip of the present invention is illustrated in **Figures 1** and **2**, which show schematically a transducer chip **10** comprising a 3x3 array of transducer elements. Those skilled in this art will recognize that the invention is not restricted to arrays of this size, but can include any two dimensional transducer array, which as used herein refers to a transducer having a plurality of elements arranged in a plurality of rows (N) and a plurality of columns (M) in a rectangular NxM grid.

Figure 1 shows three adjacent transducer elements **11, 12,** and **14,** each of which is separated from the adjacent transducer element by a kerf **13, 15.** Each kerf **13, 15** can be filled with air or with some filler material such as polymers, epoxies, glass balloons, plastic balloons, and the like. Each transducer element **11, 12, 14** is electrically connected to a corresponding connector pad **16, 18, 20.** Each of the transducer elements **11, 12,** and **14** comprises five piezoelectric layers (illustrated for element **11** as layers **24, 26, 28, 30, 32**) arranged in a vertical stack. Those skilled in this art will appreciate that although five piezoelectric layers are shown herein, any number of piezoelectric layers can be included. Each of the piezoelectric layers **24, 26, 28, 30, 32** is separated from its adjacent layers by an electrode layer (illustrated as layers **34, 36, 38, 40.** An additional electrode layer **42** contacts the lower surface **25** of the lowermost piezoelectric layer **24,** and also contacts the connector pad **16.** Likewise, an additional electrode layer **44** contacts the upper surface **33** of the uppermost piezoelectric layer **32,** and also contacts a ground plate **22** which covers all of the transducer elements.

Alternate electrode layers **42, 36,** and **40** are electrically connected by a "via" **46,** which as used herein is an electrical connection which extends through an aperture in the layers of a multilayer substrate to

electrically connect certain of the layers of the element. In the present embodiment, the via **46** extends from just beneath electrode layer **44** to electrode layer **42** and contacts electrode layers **36** and **40**, thereby connecting these layers. The via **46** is insulated from connection with electrode layers **34**, **38**, and **44** by insulation gaps **48**, **50** and **52**. In the same manner, via **54** connects electrode layers **34**, **38**, and **44** by extending along an internal surface **61** of the transducer element **11** from electrode layer **44** to an insulation gap **56** which insulates the via **54** from electrode layer **42**. As used herein, an "internal surface" of a transducer element is a surface which adjacently faces another element in another row or column across the kerf **13**, as opposed to serving as the peripheral surface of the array and thus being easily accessible for connection. Insulation gaps **58** and **60** insulate the via **54** from the electrode layers **36** and **40** respectively.

The two-dimensional nature of the transducer chip **10** can be best seen in **Figure 2**, which shows the chip at the depth of electrode layer **44**. The vias **54** each extend to and thus electrically connect this electrode layer. In contrast, the presence of the insulation gaps **52** prevents the vias **46** from electrically connecting with this electrode layer. The same configuration would be seen at electrode layers **34** and **38**. For electrode layers **42**, **36**, and **40**, the insulation gaps **56**, **58**, and **60** prevent electrical connection between the vias **54** and these electrode layer, but vias **46** do connect these electrode layers. Although they are shown herein to be located on the internal surfaces of the transducer elements, it is to be understood that the vias of the present invention can be prepositioned during fabrication so they can be located at any desired point on each element, such as an internal surface or even within the interior volume of the element. As used herein, a via which is located on an internal surface or

within the interior volume of an element is referred to as an "internal via."

The interconnection of the first set of alternating electrode layers **42, 36, 40** by a first via **46** and the interconnection by a second via **54** of a second set of alternating electrode layers **34, 38, 44** interposed between the first set of alternating electrode layers provides an element which comprises five capacitative elements connected in parallel. As a result, the capacitance of the total transducer element **11** is increased over a single piezoelectric layer of the same thickness as the total stack by the square of the number of layers; i.e., in this instance by $5^2 = 25$. Accordingly, the impedance of this element is reduced by that same factor, which improves the impedance match of these elements to electrical sources to which they are typically attached.

As those skilled in this art will appreciate, the number and thickness of piezoelectric layers in an element can vary depending on the character of the connecting device. In a preferred embodiment, the piezoelectric layers of a transducer chip **10** can be between about 0.01 and 0.15 mm in thickness, and more preferably can be between about 0.02 and 0.06 mm in thickness. As an example, to achieve a resonant frequency of 2.5MHz in a conventional 2-D array transducer, a PZT chip of thickness of about 0.6mm is required. A typical MLC-produced piezoelectric layer thickness is 0.04 mm after sintering, so K=11 layers can be easily included in a 2.5 MHz chip. Thus, the capacitance of each layer of the MLC element would be increased by a factor of 11 and the capacitance of the complete stack of 11 capacitors in parallel for a single element will be increased by $K^2=11^2=121$. The element impedance is then reduced by a factor of 121 from 5KΩ to 41Ω, an excellent match to a 50Ω electrical source.

The present invention may be used over a wide range of operating frequencies of from about 1 MHz to about 10 MHz and above. The physical dimensions and number of elements in the two-dimensional array will depend upon the application of the transducer array. For example, a square array of square transducer elements can be utilized for three dimensional imaging systems. Square transducer elements of from about 0.05 mm to about 1 mm are suitable for three dimensional imaging using frequencies of from about 10 MHz to about 1 MHz. However as smaller dimensions are utilized, operating frequencies of greater than 10 MHz may be achieved. The desired frequency of ultrasound determines the height of the chip; for example, for a 20 MHz signal, the chip can be ≈.05mm, and for a 1 MHz signal, the chip can be ≈1mm. The thickness of the chip then determines the depth of the kerf.

In an alternative embodiment, each circular via in **Figure 2** can be split, as shown in **Figures 3A** and **3B**, which illustrate electrode layers **34, 38, 44 (Figure 3A)** and electrode layers **42, 36, 40 (Figure 3B)**. The result is a transducer chip wherein a single circular via **54** can independently connect electrode layers **34, 38, 44** on the left edge of element **11 (Figure 3A)** as well as independently connecting layers **42, 36, 40** on the right edge of element **12 (3B)**. In this configuration, a single via is able to serve two independent elements. This design feature of splitting each via offers the additional advantage that one side of each split via is grounded so that two signal vias are not immediately adjacent separated only by the saw kerf. This design will reduce electrical cross talk in the piezoelectric MLC.

In an alternative embodiment to the foregoing, for fabrication reasons it may be advantageous for a split via, rather than having one half of the split via in contact with the electrode layer of one element and

the other half of the split via insulated from the same electrode layer on the adjacent element, instead to comprise halves which are mirror images of one another about a plane defined by the center of the kerf separating the adjacent elements. Thus in **Figure 3A**, via **54** would be in contact with electrode layer **34** on both element **11** and element **12**. Split via **55**, located on the other (leftmost in **Figure 3A**) surface of element **12**, would then be insulated from electrode layer **34** by an insulation gap. This pattern would continue for the other electrode layers **38, 44** in contact with electrode layer **34** and for other elements of the array. In a similar fashion, for electrode layer **36** shown in **Figure 3B**, the half of split via **54** associated with element **12** (the left half in **Figure 3B**) would be insulated from electrode layer **36** by an insulation gap which mirrors that shown for element **11**. On the leftmost edge of element **12**, the split via would be in contact with the electrode layer. The same pattern would be followed for electrode layers **42, 40**.

An additional alternative embodiment is schematically illustrated in **Figure 4** as a three-element two-dimensional array. A transducer chip **100** comprises two multilayer elements **110, 120** similar in configuration to those described above, and an element **130** comprising a single piezoelectric layer **130**. By mixing a plurality of single layer elements and plurality of multilayer elements within the same two-dimensional array, the pulse-echo sensitivity of the transducer can be improved further.

Fabrication of a MLC piezoelectric chip, which is based on computer aided design, proceeds as follows. PZT powder is mixed with organic binders, plasticizers, and solvents to form a slurry. The slurry is spread to form a thin layer and heated to form a so-called "green tape." Slurry thickness is controlled using a doctor blade technique; exemplary is a green tape thickness of

between 0.05 and 0.15 mm. Multiple holes are punched (mechanically or by laser), drilled, or etched into the tape to form the vias on each layer. The via holes are filled with a metal paste (e.g. silver or platinum) and the surface electrodes (silver or platinum paste) for each layer are laid down by screen printing excluding the insulation gaps. Multiple layers of green tape are then superimposed to align the vias, the multi-layer sandwich is laminated and then finally sintered to form a single package. Metallization is then plated or vacuum deposited on the input pads.

This transducer chip **10** then can be attached to a substrate containing electrical contact pads **16, 18** and **20** using any number of methods of bonding techniques. One such bonding technique uses conductive epoxy for a resistive contact. Another bonding technique uses a thin film approximately 1 micron thick of nonconductive epoxy for a capacitive contact. The electrical contact pads are connected to wires or vias in a multi-layer ceramic connector, traces on a circuit board, or flexible polymer circuit material. Optional conductive films can be deposited onto the piezoelectric chip **10** to produce a plurality of $\lambda/4$ matching layers to tissue.

This structure can then be divided into a plurality of transducer elements by any procedure which creates separate piezoelectric elements, such as dicing with a dicing saw. Dicing may be carried out using K & S Diamond Wheel Dicing Saw which produces kerf widths about 25 microns. The size and shape of the transducer elements is determined by the dicing pattern and is typically a square or checkerboard pattern. However other patterns such as parallelograms, circles and rhombuses may be used depending upon the specific application of the transducer array. The actual configuration of the transducer array, however, may be selected by selectively establishing electrical connections to specific transducer elements in the

checkerboard, by selective placement of connector pads or vias or by other electrical means. Active transducers may be configured by virtue of said selective connections in any number of predetermined patterns such as a cross, a filled or unfilled rectangle or a filled or unfilled circle. Note that through selection of active transducer elements, the patterns for the send transducers may be the same or different from the pattern for the receive transducers. As a final step, the ground plate **22**, usually a conductive foil, is then bonded to the piezoelectric chip **10** with a bonding agent.

An exemplary chip of the present invention formed by this method is 16 layers of PZT-5A, each layer being 0.08 mm thick, to yield a stack thickness of 1.3 mm (assuming 20 percent shrinkage during sintering). This stack has a resonant frequency of about 1.0 MHz.

Figure 5 shows an alternate embodiment of the present invention which includes a stand-off 100 to allow improved use of the present invention for medical imaging applications by allowing improved contact with the skin surface of a patient for small acoustic windows on the body such as the inter-costal space between the ribs for cardiac ultrasound diagnosis. This stand-off may be fabricated using conventional technology.

Optionally, the two-dimensional array ultrasonic transducer of the present invention may have means for redistributing the electrical connections of the connection pads **16, 18, 20** so as to increase the distance between electrical connections to a greater distance than that between individual connector pads **16, 18, 20.** This increase in spacing between electrical connections allows for simpler connection to external electronics such as voltage sources and input amplifiers. The increased spacing allows for the use of coaxial connections between the transducer array and the external electronics which results in reduced noise in the electrical output from the transducer and thereby

increases the usable sensitivity of the transducer array. The increased spacing is accomplished through conventional bond wiring, circuit boards, flexible polymer circuits, or the use of MLC technology which is illustrated and described in co-pending U.S. Patent Application Serial No. 07/883,006, the entirety of which is incorporated herein by reference.

The two dimensional array ultrasonic transducer of the present invention may also be incorporated into a handle for easier use in medical and other applications. An example of the top view of the transducer is shown in **Figure 6**, in which the interelement transducer spacing is 0.2mm so that the total footprint on the skin surface is only a 5mm x 5mm square. **Figure 7** shows the bottom view of the transducer of **Figure 6** and shows a flange containing a pad array for connection to an optional transducer handle. The inter-element spacing of the pads is 0.635mm so that a redistribution, or fan-out, occurs in the connector, thereby enabling easier electrical connection to the cables of the transducer handle.

Uses for the present invention include three dimensional ultrasound imaging or volumetric measurements and thin slice ultrasound imaging. In use, the transducer elements of the two-dimensional array ultrasonic transducer are excited by a voltage source in electrical connection with the transducer elements through the connector. The electrical voltage source places an electrical voltage across the element to produce an ultrasonic output from the element. These voltages typically range from about 50 volts to about 300 volts. The voltage excites the transducer element to produce an ultrasonic signal which is transmitted from the transducer array into a test region. When receiving ultrasonic signals, the ultrasonic signal excites a transducer element to produce an electrical voltage across the transducer element. This electrical voltage is then amplified by an amplifier in electrical

connection with the transducer element through the connector. A further advantage of the present invention is the ability to use what is known in the art as "cavity down" positioning of an integrated circuit with the connector to provide amplifiers for receive and transmit mode use of the transducers in a single integrated package. Using the "cavity down" method, an integrated circuit is mounted directly onto the connection side of the multilayer ceramic connector thereby incorporating the integrated circuit as part of the transducer array assembly and allowing for the integration of the circuitry into the handle of the transducer array to provide a more compact unit.

Figure 8 shows a block diagram of a phased array medical ultrasonic scanner **140**. The scanner includes transmitter circuitry **150**, a transducer array **160** of the present invention, receiver amplifier circuitry **170**, signal processing circuitry **180**, such as envelope detection and filtering, a scan converter **190**, and a television monitor **200**.

The foregoing is illustrative of the present invention and is not to be construed as limiting thereof. For example, other methods of fabrication of the present invention may be utilized while still benefitting from the teachings of the present invention. Those skilled in this art will also appreciate that other methods of increasing the distance between electrical connections to the transducer elements of the present invention may be utilized. The invention is accordingly defined by the following claims, with equivalents of the claims to be included thereof.

CLAIMS:

1. A piezoelectric transducer chip comprising:

a plurality of transducer elements of a width of from about 0.05 mm to about 1 mm arranged in a two-dimensional array, at least one of said transducer elements being a multilayer element having an internal edge portion and comprising a plurality of piezoelectric layers and a plurality of electrode layers forming a plurality of capacitative elements electrically connected in parallel, each of said plurality of piezoelectric layers being separated from the adjacent piezoelectric layers by one of said plurality of electrode layers, and said piezoelectric layers consisting of a first set of alternating electrode layers and a second set of alternating electrode layers interposed between said first set of alternating electrode layers;

a first via electrically connecting said first set of alternating electrode layers, said first via being electrically insulated from said second set of alternating electrode layers; and

a second via electrically connecting said second set of alternating electrode layers, said second via being electrically insulated from said first set of alternating electrode layers;

wherein at least one of said vias is an internal via.

2. A piezoelectric transducer chip according to claim 1, wherein said plurality of transducer elements comprises a plurality of multilayer elements.

3. A piezoelectric transducer chip according to claim 1, wherein said multilayer element comprises piezoelectric layers which are between about 0.01 and 0.6 mm in thickness.

4. A piezoelectric transducer chip according to claim 1, wherein said multilayer element is substantially square in cross-section.

5. A piezoelectric transducer chip according to claim 1 wherein said first set of alternating electrode layers and said second set of alternating electrode layers each comprise a plurality of electrode layers.

6. A piezoelectric transducer chip according to claim 1, wherein said first via is insulated from said second set of alternating electrodes by a plurality of insulating gaps.

7. A piezoelectric transducer chip according to claim 1, wherein said second via is insulated from said first set of alternating electrodes by a plurality of insulating gaps.

8. A piezoelectric transducer chip according to claim 1, wherein said multiple layer elements are rectangular in cross-section.

9. A piezoelectric transducer chip according to claim 1, wherein at least one of said transducer elements has a single piezoelectric layer

10. An ultrasonic transducer array comprising:

(a) a connector having an upper surface, a lower surface, and an array of connector pads formed in said connector for electrically connecting said upper surface to said lower surface;

(b) a piezoelectric transducer chip having a plurality of ultrasonic transducer elements arranged in a two-dimensional array, at least one of said ultrasonic transducer elements being a multilayer element having an

internal edge portion and comprising a plurality of piezoelectric layers and a plurality of electrode layers forming a plurality of capacitative elements electrically connected in parallel, each of said plurality of piezoelectric layers being separated from the adjacent piezoelectric layers by one of said plurality of electrode layers, and said piezoelectric layers consisting of a first set of alternating electrode layers and a second set of alternating electrode layers interposed between said first set of alternating electrode layers;

(c) a first via connecting said first set of alternating electrode layers, said first via being electrically insulated from said second set of alternating electrode layers; and

(d) a second via connecting in parallel said second set of alternating electrode layers, said second via being electrically insulated from said first set of alternating electrode layers;

wherein at least one of said vias is an internal via;

(e) means for electrically connecting said first set of alternating electrodes to ground; and

(f) means for electrically connecting said second set of alternating electrodes to a corresponding one of said connector pads.

11. An ultrasonic transducer array according to claim 10, which further comprises a metallic ground sheet which overlies said piezoelectric transducer chip and is electrically connected to said means for electrically connecting said first set of alternating electrodes.

12. An ultrasonic transducer array according to claim 10, wherein said means for electrically connecting said second set of alternating electrodes

comprises a bonding layer to connect to said upper surface of said connector.

13. An ultrasonic transducer array according to claim 10, wherein said piezoelectric chip comprises a plurality of multilayer elements.

14. An ultrasonic transducer array according to claim 10, wherein said piezoelectric chip comprises at least one multilayer element which includes a first internal edge and a second internal edge, and wherein said first via is an internal via, and wherein said second via is an internal via.

15. An ultrasonic transducer array according to claim 10, wherein said ultrasonic transducer operates at a frequency of between about 1 and 10 MHz.

16. An ultrasonic scanner comprising:

(a) means for producing an ultrasonic signal;

(b) an ultrasonic transducer array operatively connected to said means for producing an ultrasonic signal for transmitting said ultrasonic signal to a target said ultrasonic transducer array comprising:

(i) a connector having an upper surface, a lower surface, and an array of connector pads formed in said connector for electrically connecting said upper surface to said lower surface;

(ii) a piezoelectric transducer chip having a plurality of ultrasonic transducer elements arranged in a two-dimensional array, at least one of said ultrasonic transducer elements being a multilayer element having an internal edge portion and comprising a plurality of piezoelectric layers and a plurality of electrode layers forming a

plurality of capacitative elements electrically connected in parallel, each of said plurality of piezoelectric layers being separated from the adjacent piezoelectric layers by one of said plurality of electrode layers, and said piezoelectric layers consisting of a first set of alternating electrode layers and a second set of alternating electrode layers interposed between said first set of alternating electrode layers;

(iii) a first via connecting said first set of alternating electrode layers, said first via being electrically insulated from said second set of alternating electrode layers; and

(iv) a second via connecting in parallel said second set of alternating electrode layers, said second via being electrically insulated from said first set of alternating electrode layers;

wherein at least one of said vias is an internal via;

(v) means for electrically connecting said first set of alternating electrodes to ground; and

(vi) means for electrically connecting said second set of alternating electrodes to a corresponding one of said connector pads;

(c) means for amplifying a received ultrasonic signal from a target operatively connected to said ultrasonic transducer array; and

(d) means for processing said ultrasonic signal operatively connected to said amplifying means.

17. An ultrasonic transducer array according to claim 16, which further comprises a metallic ground sheet which overlies said piezoelectric transducer chip and is electrically connected to said means for

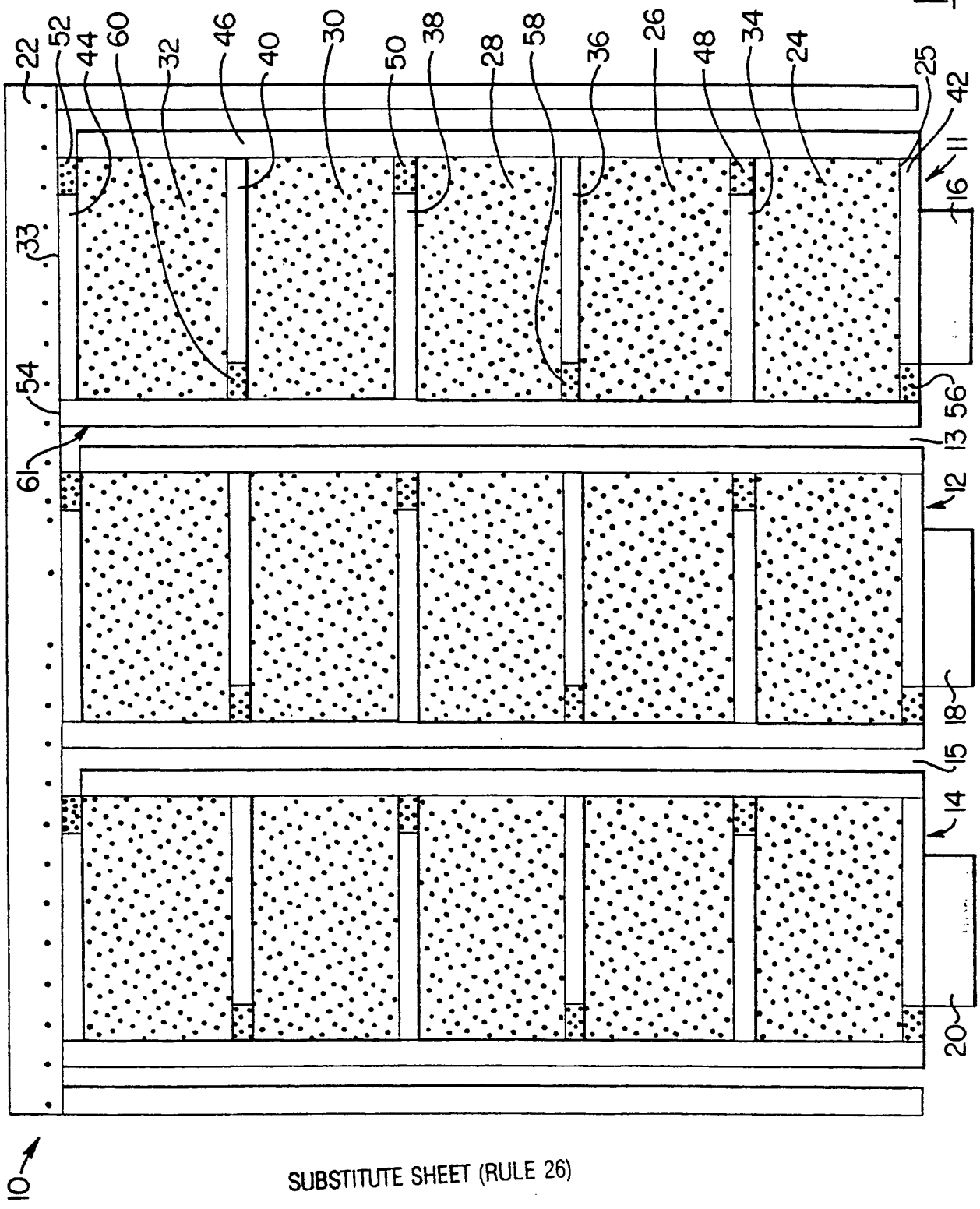
electrically connecting said first set of alternating electrodes.

18. An ultrasonic transducer array according to claim 16, wherein said means for electrically connecting said second set of alternating electrodes comprises a bonding layer to connect to said upper surface of said connector.

19. An ultrasonic transducer array according to claim 16, wherein said piezoelectric chip comprises a plurality of multilayer elements.

20. An ultrasonic transducer array according to claim 16, wherein said piezoelectric chip comprises at least one multilayer element which includes a first internal edge and a second internal edge, and wherein said first via is an internal via, and wherein said second via is an internal via.

FIG. 1.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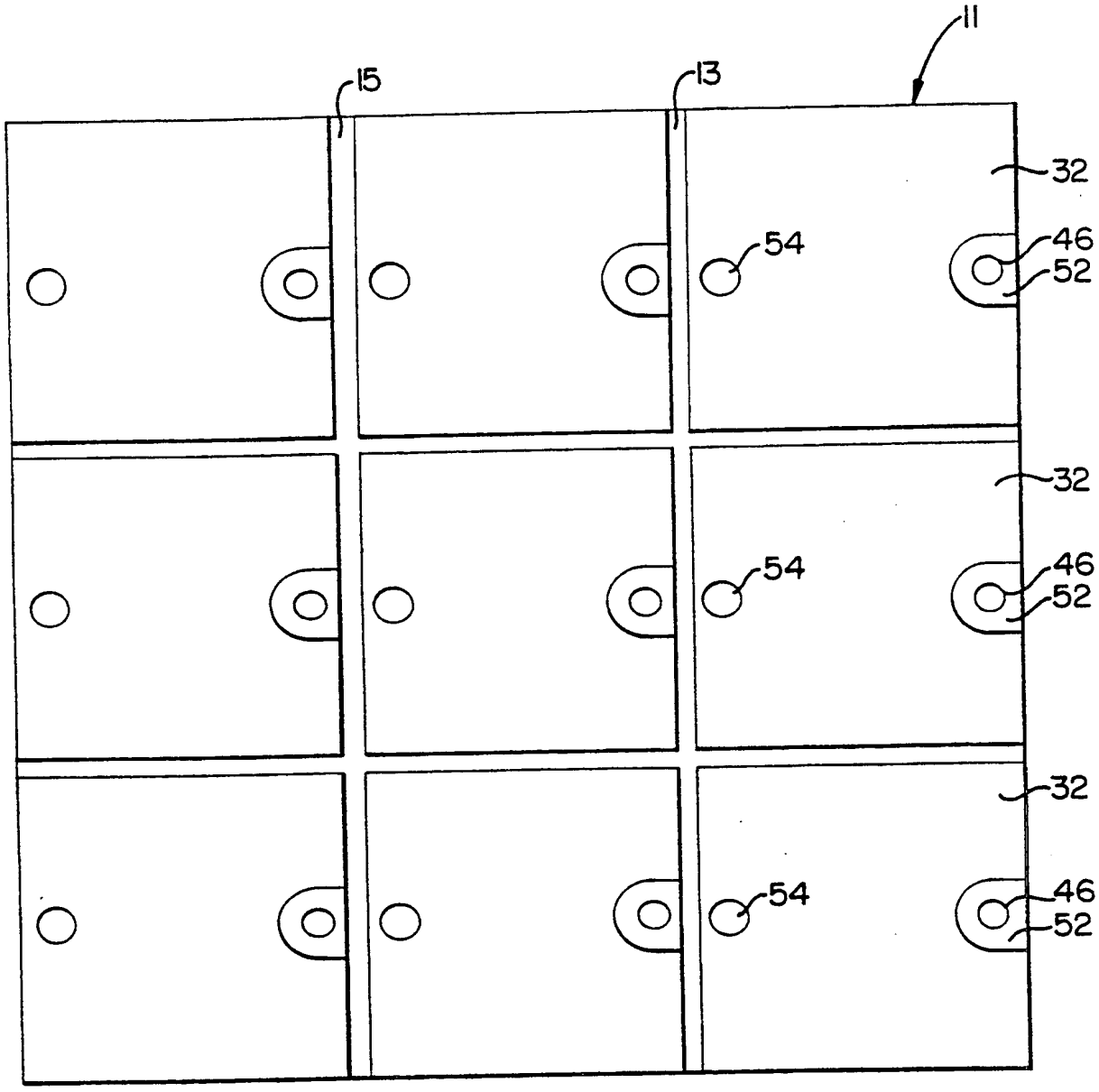


FIG. 2.

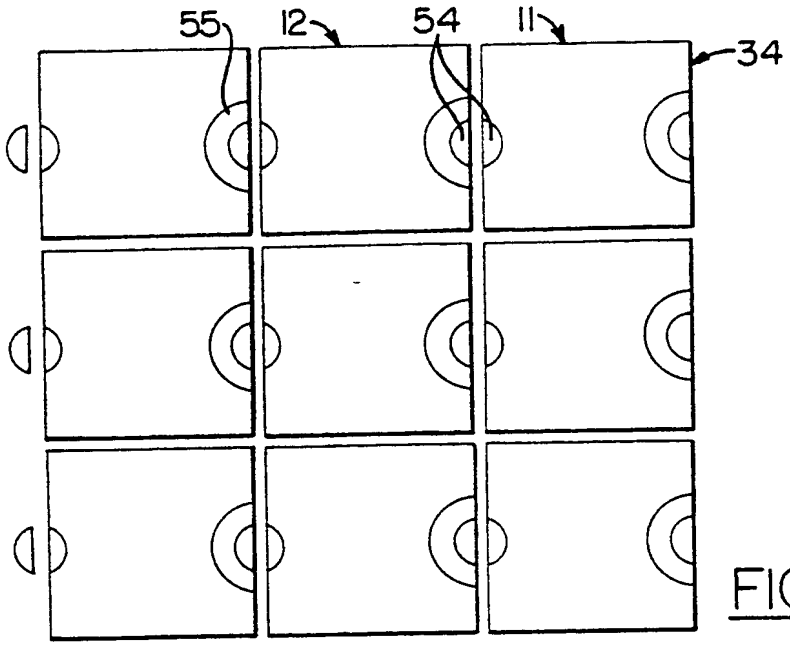


FIG. 3A.

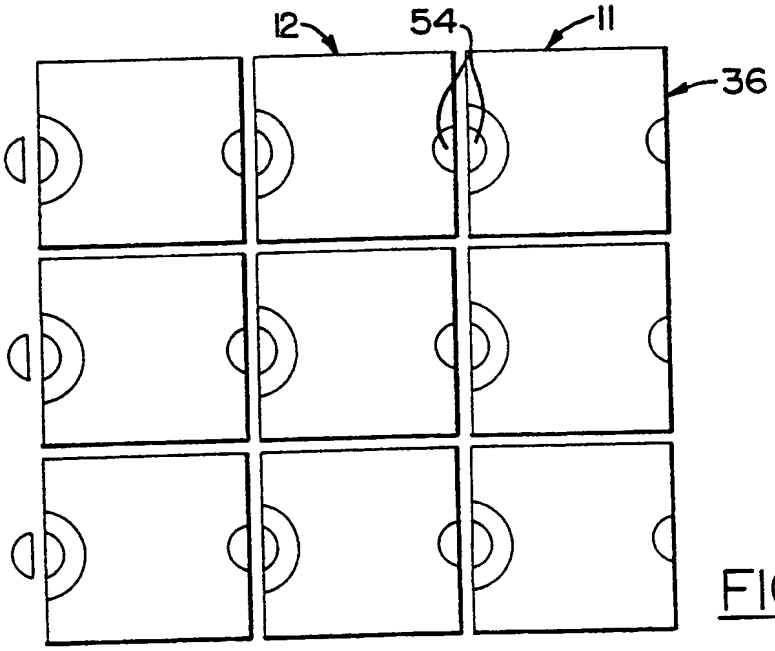
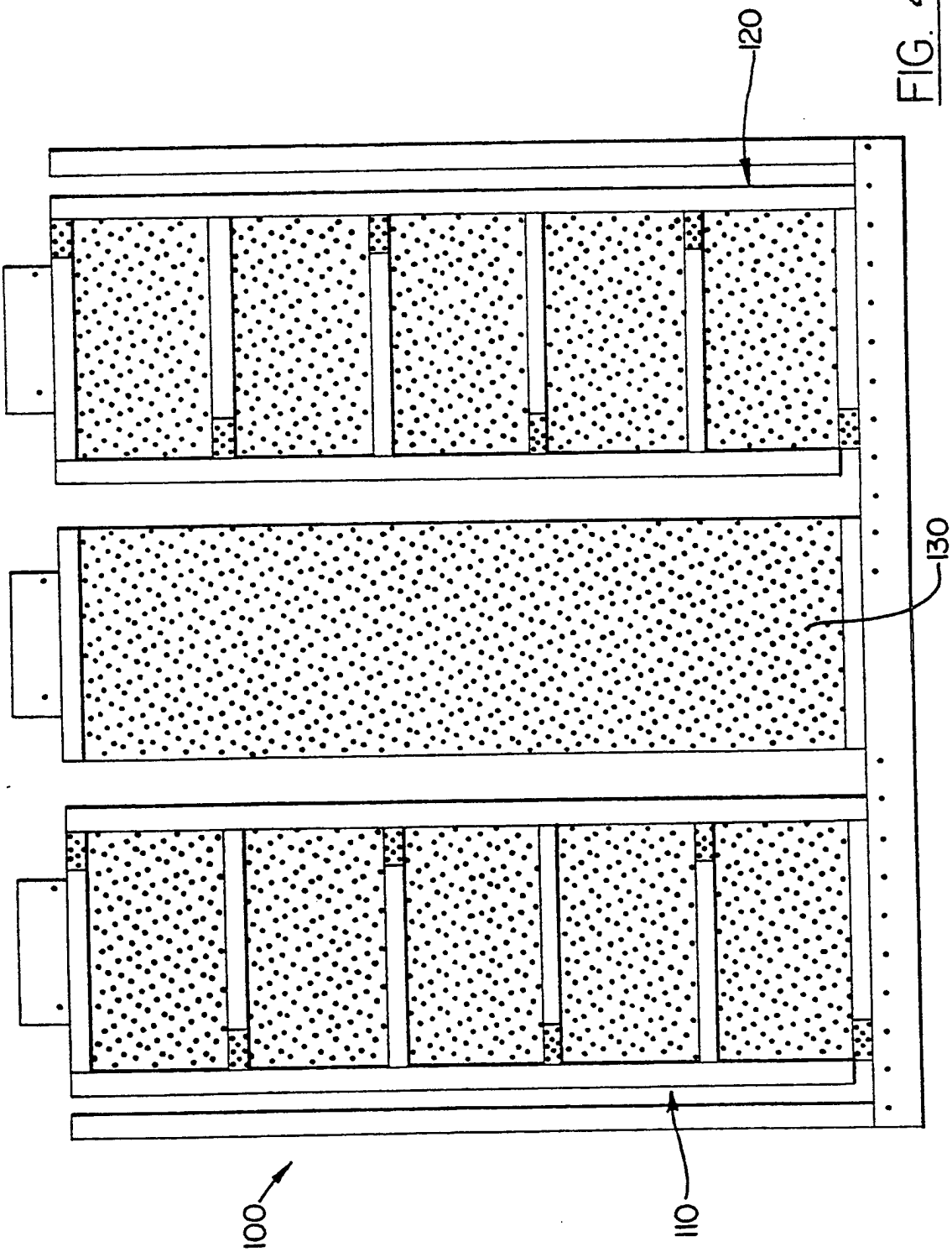


FIG. 3B.

FIG. 4.



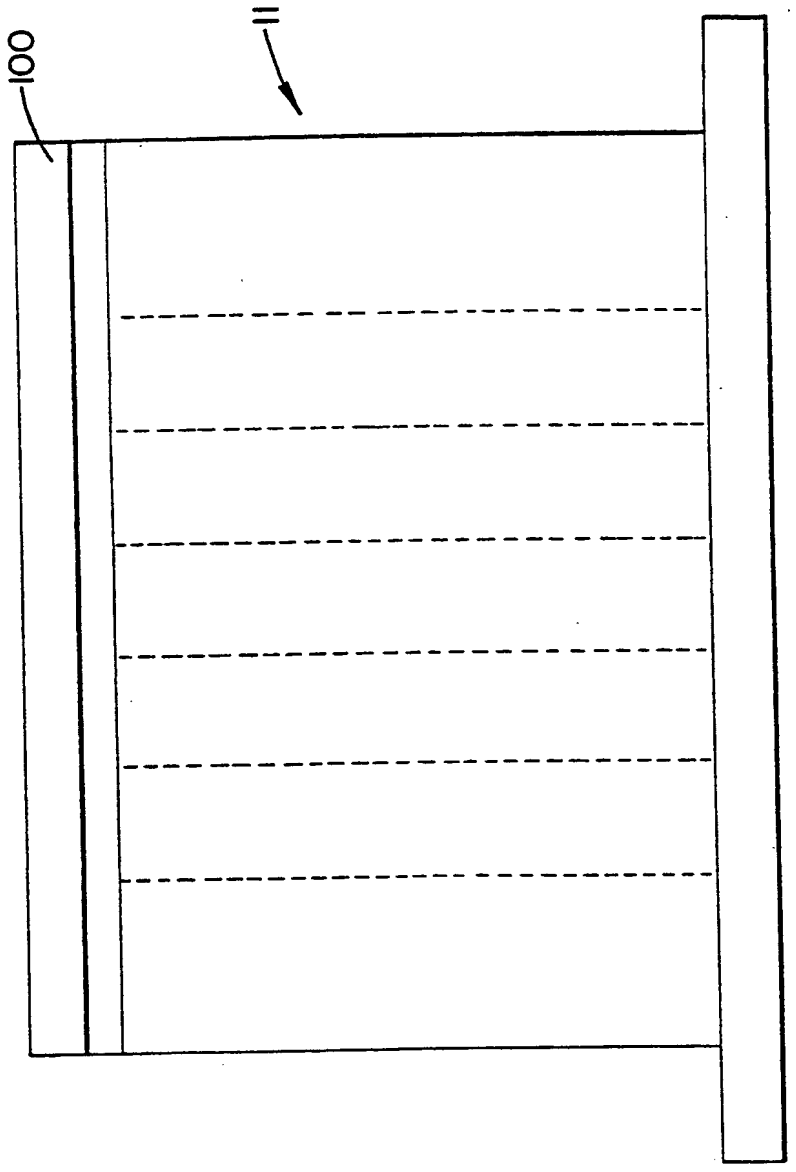


FIG. 5.

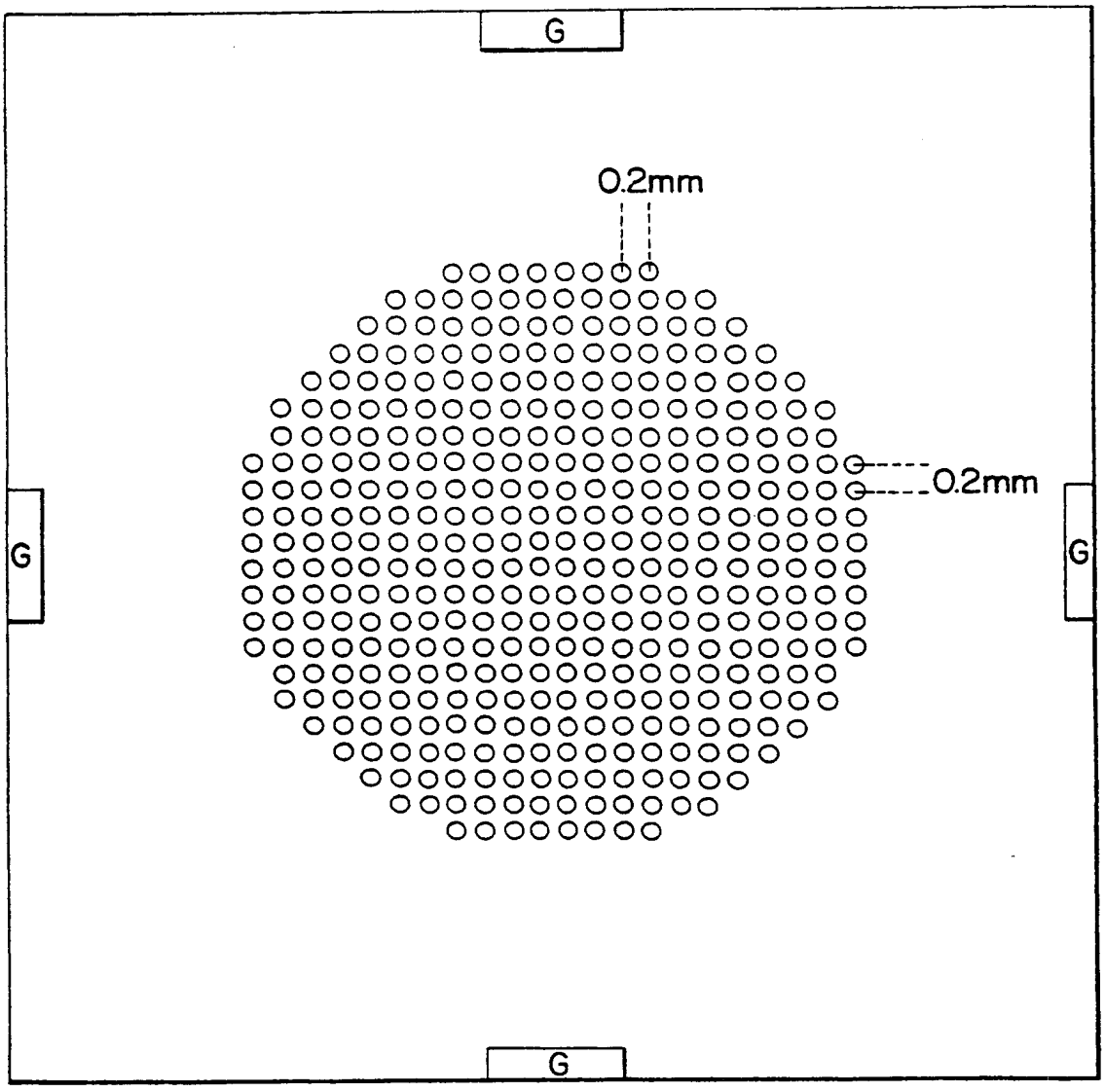


FIG. 6.

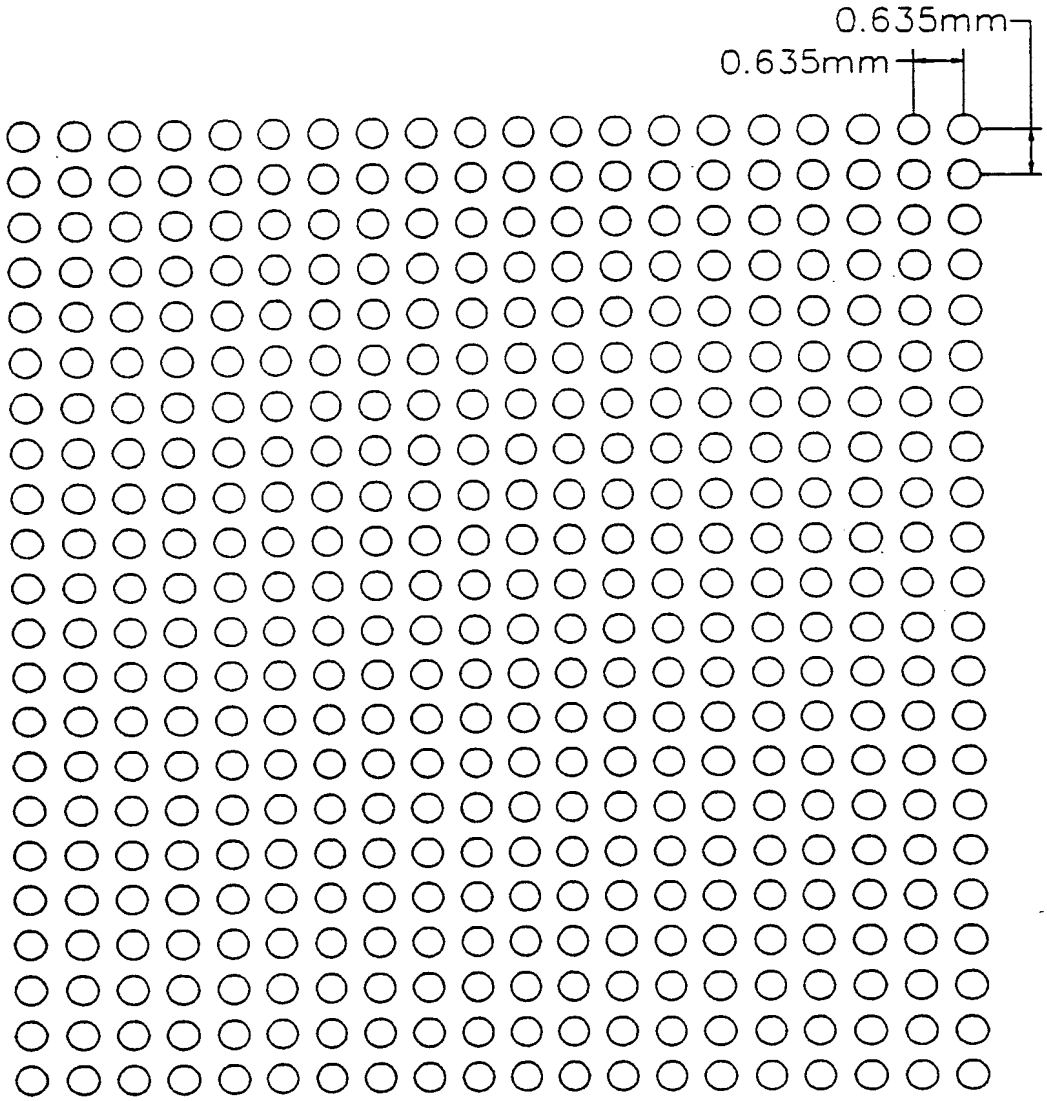


FIG. 7.

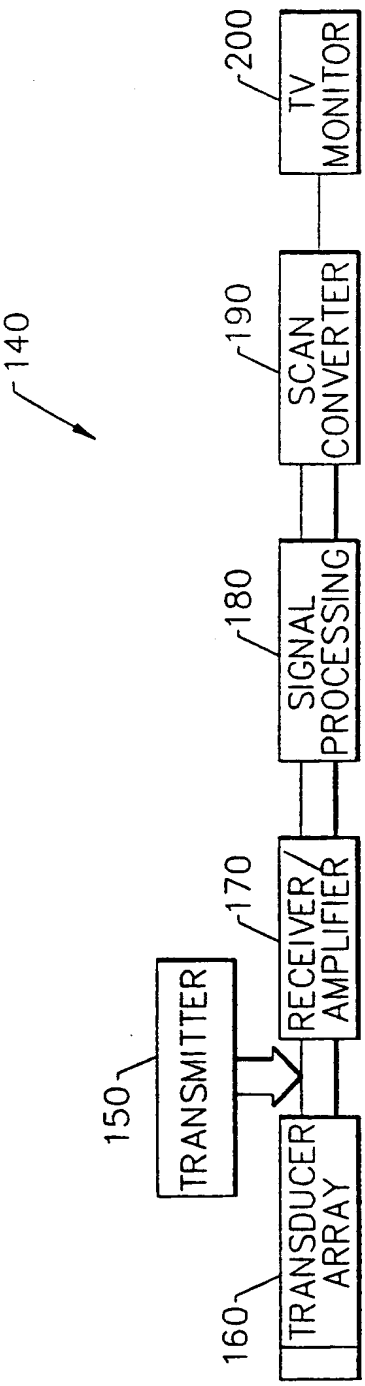

140
200
TV MONITOR
190
SCAN CONVERTER
180
SIGNAL PROCESSING
170
RECEIVER/ AMPLIFIER
150
TRANSMITTER
160
TRANSDUCER ARRAY

FIG. 8.

INTERNATIONAL SEARCH REPORT

In ational application No.
PCT/US93/09520

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H04R 17/00

US CL : 367/140, 155; 310/334, 336; 128/662.03

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 367/140, 155, 153; 310/334, 336, 364; 128/662.03, 661.01, 663.01, 660.01

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,211,948 (Smith et al) 08 July 1980, See entire document	1-20
A	US,A, 4,217,684 (Brisken et al) 19 August 1980, See entire document.	1-20
A	US,A, 4,296,349 (Nakanishi et al) 20 October 1981, See entire document.	1-20
A	US,A, 4,489,729 (Sorenson et al) 25 December 1984, See entire document.	1-20
A	US,A, 4,603,276 (Coursant) 29 July 1986, See entire document	1-20
A	US,A, 4,638,468 (Francis) 20 January 1987, See entire document.	1-20

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

01 JANUARY 1994

Date of mailing of the international search report

FEB 28 1994

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INTERNATIONAL SEARCH REPORT

In ational application No.
PCT/US93/09520

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,773,140 (McAusland) 27 November 1988, See entire document.	1-20
A	US, A, 4,755,708 (Granz et al) 05 July 1988, See entire document.	1-20
A	US,A, 4,747,192 (Rokurota) 31 May 1988, See entire document	1-20
A	US,A, 4,890,268 (Smith et al) 26 December 1989, See entire document.	1-20
A	US, A, 4,945,915 (Nagasaki et al) 07 August 1990, See entire document	1-20
A	US,A, 4,958,227 (Saitoh et al) 18 September 1990, See entire document.	1-20
A	US,A, 5,014,711 (Nagasaki et al) 14 May 1991, See entire document.	1-20
A	US,A, 5,045,746 (Wersing et al) 03 September 1991, See entire document.	1-20
A	US,A, 5,091,893 (Smith et al) 25 February 1991, See entire document.	1-20
A	US,A, 4,865,042 (Umemura et al) 12 September 1989, See enitre document	1-20